SELECTIVE METAL OXIDE REMOVAL

Related Applications

This application is related to the following applications that are assigned to the assignee hereof:

U.S. Patent Application serial number 09/851,206, by Hobbs et al., entitled "Method for Making a Semiconductor Device;" and

U.S. Patent Application serial number 09/574, 732, by Hobbs et al., entitled "Selective Removal of a Metal Oxide Dielectric."

Background of the Invention

In developing high-k dielectrics for use as gate insulating layers, the most common type of such high-k dielectrics have been metal oxides. These metal oxides have a significant higher dielectric constant than the historic gate insulator of silicon oxide. In developing these metal oxides it has become a problem of doping the source/drain with implants through such metal oxides. Thus, implanting through these metal oxides has been difficult because the metal oxides absorb and impede the progress of the dopants that are being implanted. This can result in shallower source/drain regions, which is undesirable, and also in the PN junctions being less abrupt. The energy of the implant can be increased to achieve the desired depth of the source/drains but the abruptness of the PN junctions that are formed is still reduced. The disadvantage of PN junctions that are not abrupt is increased resistance of the doped region due to the larger areas of low concentration of doping and also higher current leakage. The higher current leakage may result from the depletion region extending further and enclosing more areas that have defects.

Further, the metal oxide must ultimately be removed in order to make contact to the source/drains.

To overcome this disadvantage of implanting through a metal oxide, there have been attempts to remove the metal oxide prior to performing the source/drain implants. Removal of this metal oxide, however, has been very difficult to control. If the etch of the metal oxide continues for too long, the underlying interfacial oxide is removed and the underlying silicon is pitted. Thus there is a need to provide a technique for removing metal oxides that does not result in pitting this silicon substrate.

Brief Description of the Drawings

The present invention is illustrated by way of example and not by limitation in the accompanying figures, in which like references indicate similar elements, and in which:

Shown in FIG. 1-7 are sequential cross-sections of a portion of a semiconductor wafer according to a preferred embodiment of the invention; and

Shown in FIG. 8 is an apparatus useful in performing a portion of the method used in achieving the cross-sections shown in FIGs. 1-7.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

Description of the Invention

In an embodiment of the invention a selective removal of a metal oxide is achieved by flowing anhydrous HCl (HCl) over a metal oxide layer while it is receiving heat by radiation. The metal oxide is effectively removed while the interfacial oxide layer underlying a gate electrode is retained and protects the underlying silicon. The HCl flows across the wafer in the absence of being energized by high frequency electromagnetic waves. In this case, high frequency means radio frequency or microwave radiation and is conveniently referenced as "rf" herein.

Shown in FIG. 1 is a device structure 10 comprising a silicon substrate 12, an interfacial oxide layer 14, a metal oxide layer 16, a gate electrode 18, and an antireflective coating (ARC) 20. The area immediately under gate electrode 18 is the critical area for having a high degree of coupling and is the area where it is important for the interfacial oxide layer 14 to be thin. Metal oxide layer 16 is preferably hafnium oxide and is about 30 angstroms in thickness. Gate electrode 18 may be any appropriate gate material and is preferably polysilicon. ARC 20 is any appropriate antireflective coating material and is preferably silicon-rich nitride. The interfacial oxide layer 14 is much thinner under gate electrode 18 than in source/drain areas not under gate electrode 18. Gate electrode 18 acts as a mask to oxygen and thus prevents additional growth of interfacial oxide layer 14 in the area under the gate electrode.

Shown in FIG. 2 is device structure 10 after removal of metal oxide 16 in areas other than those under gate electrode 18. The portion of metal oxide 16 which remains is shown as metal oxide 22 which is present only under gate

electrode 18. Metal oxide 16 is selectively removed by placing it in a reaction chamber such as that shown in FIG. 8.

Shown in FIG. 8 is an apparatus 26 comprising a reaction chamber 24, a source of hydrogen chloride 28, a support 30, a radiation source 32, and a wafer 34 that has device structure 10 present therein. Wafer 34 is placed on support 30 and receives heat from radiation source 32. Coincident with wafer 34 receiving this radiation, HCl is flowed over wafer 34. There is no rf energy applied to the HCl. The result is the removal of the metal oxide 16 that is exposed and the retention of interfacial oxide layer 14. It has been found that an effective range of heat for wafer 34 is 600-800 degrees C. Even higher temperatures may be useful, especially with very low partial pressures of HCl. As the temperature increases to the high end of that range, there tends to be more removal of the metal oxide under gate electrode 18. This would be the type of undercutting that is commonly associated with isotropic etching. At the lower end of this range the removal of the metal oxide is slow. A good temperature that has been found to be effective in providing a good rate of removal of the metal oxide and minimal undercutting of the metal oxide under gate electrode 18 is a temperature of 650 degrees C. A good range of operation has been found to be 625-675 degrees C. The combination of the radiation and the HCl is applied for about 60 seconds at a pressure of 50 torr and at a flow rate one standard liter per minute (SLM). Also flowing with the HCl is 9 SLM of nitrogen (N_2), which operates as an inert gas. Other inert gases may also be effective.

Other combinations of time, temperature, pressure and flow rate may also be found to be effective for effective removal of the metal oxide without significant undercutting. In practice, the HCl is flowed prior to the application

of the heat from the radiation source 32. As an alternative, heat could be achieved by convection or contact between a hot plate, for example, instead of by radiation as shown in FIG. 8. An advantage of radiation heating is that it provides for relatively faster ramp up times and ramp down times.

Shown in FIG. 3 is device structure 10 after removal of ARC layer 20. ARC 20 may be removed by a dry etch or a wet etch. A dry etch may result in some bombardment of the sacrificial oxide layer 14, which is exposed, and potentially even reaching the silicon of substrate 12. This possibility may be avoided by using a wet etch. Another possibility is to remove ARC 20 prior to the selective removal of metal oxide 16. Hot phosphoric acid is an effective wet etch for an ARC layer made of silicon rich silicon nitride.

Shown in FIG. 4 is device structure 10 after a short, wet dip of device structure 10 into hydrofluoric acid (HF). The purpose of the HF dip is to clean up any accumulated metal present in interfacial oxide 14 by removing interfacial oxide 14 to leave thin interfacial oxide layer 25 under gate electrode 18. The time is about 30 seconds. The time can be adjusted according to the concentration of the HF. It should be long enough to insure the removal of the interfacial oxide layer 14 but not so long as to roughen the underlying silicon of substrate 12. The interfacial oxide layer 14 in the area that is not under gate electrode 18 is in the range of about 15-35 angstroms. After the HF dip, the device structure 10 is rinsed with de-ionized water and may be exposed to air. The result is shown in FIG. 5 with device structure 10 then having an interfacial oxide layer 27 in the area not under gate electrode 18 having a thickness in the range of about 8-15 Angstroms.

Shown in FIG. 6 is device structure 10 after two implants. One of the implants is known as a halo implant and forms regions 40 and 42. The other

implants are the source drain extension implants and form source drain regions 44 and 46. Regions 44 and 46 are of the opposite conductivity type of that of substrate 12 whereas halo regions 40 and 42 are of the same conductivity type as substrate region 12. Substrate 12 is representative of either P-wells or N-wells and may be over an insulating layer as is common for substrates known as SOI. Halo regions 40 and 42 are to improve punchthrough.

Shown in FIG. 7 is device structure 10 after formation of sidewall spacers 48 and 50 and the heavy source/drain implant. The heavy source/drain implant results in heavily doped contact regions 52 and 54. Portions of regions 52 and 54 immediately adjacent to the area immediately under gate electrode 18 are comparatively lightly doped. The doping of regions 54 and 52 is a significantly higher concentration than the doping of regions 40 and 42. Device structure 10 as shown in FIG. 7 is thus a completed transistor.

Anhydrous halides other than HCl may provide similar results. Gaseous HF for example may remove the metal oxide effectively under similar conditions. A disadvantage of HF with respect to HCl is that HF is much less selective to silicon oxide. Thus, the interfacial oxide 14, after the metal oxide was penetrated, would be removed at a greater rate with HF than it would be with HCl. Also metal fluorides are less volatile than metal chlorides which may result in less effective removal of the metal oxide. Thus, HCl is considered to be more desirable for use than gaseous HF. Other exemplary gaseous halides that may be effective are HI, HBr, I_2, Br_2, Cl_2, and F_2. Hafnium oxide has a particular advantage as a high-k dielectric as being stable with respect to polysilicon. It is less reactive with the polysilicon at the time the polysilicon is deposited compared to many other high-k dielectrics.

The absence of rf activation of the HCl has been found to be advantageous. A typical plasma etch, which uses rf, that included chlorine gases was found to pit the substrate. The pitting is believed to be a result of bombardment, physical etching as distinguished from chemical etching, of the surface by the rf-energized chlorine. The absence of the rf provides for just chemical removal of the metal oxide. This chemical removal of the present invention is believed to work by causing a reaction between the gaseous halide, preferably HCl, and the metal oxide to generate a byproduct of a portion of the HCl and the metal in the metal oxide. Also the byproduct is volatile so that it is easily removed from the reaction chamber and away from the wafer. This successful avoidance of the pitting is very beneficial because pitting can result in non-uniform implant doping, which results in increased resistance and/or other degradation in transistor performance.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.